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# ENHANCEMENT OF FORWARD BIASED LED CURRENT FOR LED DERIVER IC

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## ABSTRACT

The Light-Emitting Diode (LED) driver is an important part of Visible Light Communication (VLC) systems. The main challenge of the VLC LED driver is to offer a high data transmission rate with high power efficiency. This paper presents the design of a white light LED driver that combines the LED lighting with VLC technology. The proposed LED driver uses linear current regulation and controls the AC current signal and the DC current through a single power device for the purposes of high speed, high efficiency and high integration. It also can support the modulation format of orthogonal frequency division multiplexing (OFDM). In addition, this work presents an impedance reduction technique to enhance the bandwidth of the LED driver. And a first-order pre-equalizer is utilized to enhance the electron-optical-electron (E/O/E) bandwidth in the VLC system due to the bandwidth limitation of the phosphor converted LED. The VLC LED driver is fabricated in a standard 0.5_m CMOS technology with chip area 1540_m×1250_m. It is available in a standard SOP-16 pin package. The experimental results show that the optical modulation bandwidth of 10.9 MHz has been achieved with the forward biased LED current of 350 mA. By using the OFDM data modulation scheme, the data rate of 50 Mb/s is demonstrated.

## INTRODUCTION

MOS transistor based integrated circuits have transformed the world we live in. It is estimated that there are more than 15 billion silicon semiconductor chips currently in use with an additional 500,000 sold each day. The ever shrinking size of the MOS transistors that result in faster, smaller, and cheaper systems have enabled ubiquitous use of these chips. Among these semiconductor chips, a prevalent component is the high-performance general-purpose microprocessor. The timeline on technology scaling and new high-performance microprocessor architecture introductions in the past three decades. This trend holds in general for other segments of the semiconductor industry as predicted by Moore's law. In 1965, Gordon Moore showed that for any MOS transistor technology there exists a minimum cost that maximizes the number of components per integrated circuits. He also showed as transistor dimensions are shrunk (or scaled) from one technology generation to the next, the minimal cost point allows significant increase of the number of components per integrated circuit historically, technology scaling resulted in scaling of vertical and lateral dimensions by 0.7X. .each generation resulting in delay of the logic gates to be scaled by 0.7X and the integration density of logic gates to be increased by 2X. From the timeline shown in Figure 1-1 it is clear that there were two distinct eras in technology scaling – constant voltage scaling and constant electric field scaling.

## CONVENTIONAL CMOS TECHNOLOGY

Conventionally, CMOS technology has been scaled to provide 30% smaller gate delay with 30% smaller dimensions, resulting in CMOS systems operating at about 40% higher frequency in half the area with reduced energy consumption. Scaled CMOS systems, such as new generation microprocessors, achieve at least an additional 60% frequency increase with augmented architecture and circuit techniques. This complexity increase results in higher energy consumption, peak power dissipation and power delivery requirements.

## TECHNOLOGY SCALING AND THRESHOLD VOLTAGE VARIATION

With technology scaling, the MOSFET's channel length is reduced. As the channel length approaches the source-body and drain-body depletion widths, the charge in the channel due to these parasitic diodes become comparable to the depletion charge due to the MOSFET gate-body voltage [1], rendering the gate and body terminals to be less effective. As the band diagram illustrates in Figure 2-1, the finite depletion width of the parasitic diodes do not influence the energy barrier height to be overcome for inversion formation in a long channel device. However, as the channel length becomes shorter both channel length and drain voltage reduce this barrier height. This two- dimensional effect makes the barrier height to be modulated by channel length variation resulting in threshold voltage variation as shown in Figure 2-2. The amount of barrier height lowering, threshold voltage variation, and gate and body terminal's channel control loss will directly depend on the charge contribution percentage of the parasitic diodes to the total channel charge. Figure 2-3 shows measurements of 3 threshold voltage variations for three device lengths in a 0.18microm. technology confirming this behavior. It is

essential to mention that in sub-micron technologies variation in several physical and process parameters lead to variation in the electrical behavior of the MOS device.
The discussions in this thesis will address variation in the electrical behavior manifested as threshold voltage variation because of parameter variation. In addition, the threshold voltage variations addressed here are due to short channel effect in scaled MOS devices and not on Threshold voltage variation due to random dopant fluctuation effect. Random dopant fluctuation effect is expected to be one of the significant sources of threshold voltage variation in devices of small area [2].

## DESIGN MEMORY UNIT

At the same time, as VLSI design sizes and their operating frequencies continue to increase, timing-related defects are high proportion of the total chip defects and at speed test is crucial. DFT techniques are widely used in order to improve the testability of a design. While DFT techniques facilitate generation and application of tests, they may cause the test vectors to contain non-functional states which result in higher switching activities compared to the functional mode of operation. Excessive switching activity causes higher power dissipation as well as higher peak supply currents. Excessive power dissipation may cause hot spots that could cause damage the circuit. Excessive peak supply currents may cause higher IR drops which increase signal propagation delays during test causing yield loss. Several methods have been proposed to reduce the switching activity in the circuit under test during shift and capture cycles. While these methods reduce switching activity during test and eliminate the abnormal IR drop, circuits may now operate faster on the tester than they would in the actual system. For speed related and high resistance defect mechanisms, this type of under testing means that the device could be rejected by the systems integrator or by the end consumer and thus increasing the DPPM of the devices. Therefore, it is critical to ensure that the peak switching activity generated during the two functional clock cycles of an at-speed test is as close as possible to the functional switching activity levels specified for the device.

In portable electronic devices that operate on battery power, it is essential to have power saving techniques to increase the operating time as they are energy constrained. This paper presents a novel power saving technique supported by two design models for multimedia purposes. The two designs are with two varying significance. The most significant part is turned off when it can't produce different results. This is done to save power consumption. The two design examples explored in this paper have varying hardware configurations thus reveal different realization. The models are namely multi-transform model and multimedia Functional unit. The former computes three transforms for H.264 encoding while the latter supports six functions which are commonly used namely addition, multiplication, subtraction, interpolation, MAC and sum-of absolute-difference. For these designs the proposed VLSI technique is capable of saving power by 27% and 24% respectively at the expense of 20% area overheads.

## SEMICONDUCTOR DEVICE MODELING

The physics and modeling of devices in integrated circuits is dominated by MOS and bipolar transistor modeling. However, other devices are important, such as memory devices that have rather different modeling requirements. There are of course also issues of reliability engineering—for example, electro-static discharge (ESD) protection circuits and devices—where substrate and parasitic devices are of pivotal importance. These effects and modeling are not considered by most device modeling programs; the interested reader is referred to several excellent monographs in the area of ESD and I/O modeling.

Physics driven device modeling is intended to be accurate, but it is not fast enough for higher level tools, including circuit simulators such as SPICE. Therefore, circuit simulators normally use more empirical models (often called compact models) that do not directly model the underlying physics. For example, inversion-layer mobility modeling, or the modeling of mobility and its dependence on physical parameters, ambient and operating conditions is an important topic both for TCAD (technology computer aided design) physical models and for circuit-level compact models. However, it is not accurately modeled from first principles, and so resort is taken to fitting experimental data. For mobility modeling at the physical level the electrical variables are the various scattering mechanisms, carrier densities, and local potentials and fields, including their technology and ambient dependencies.

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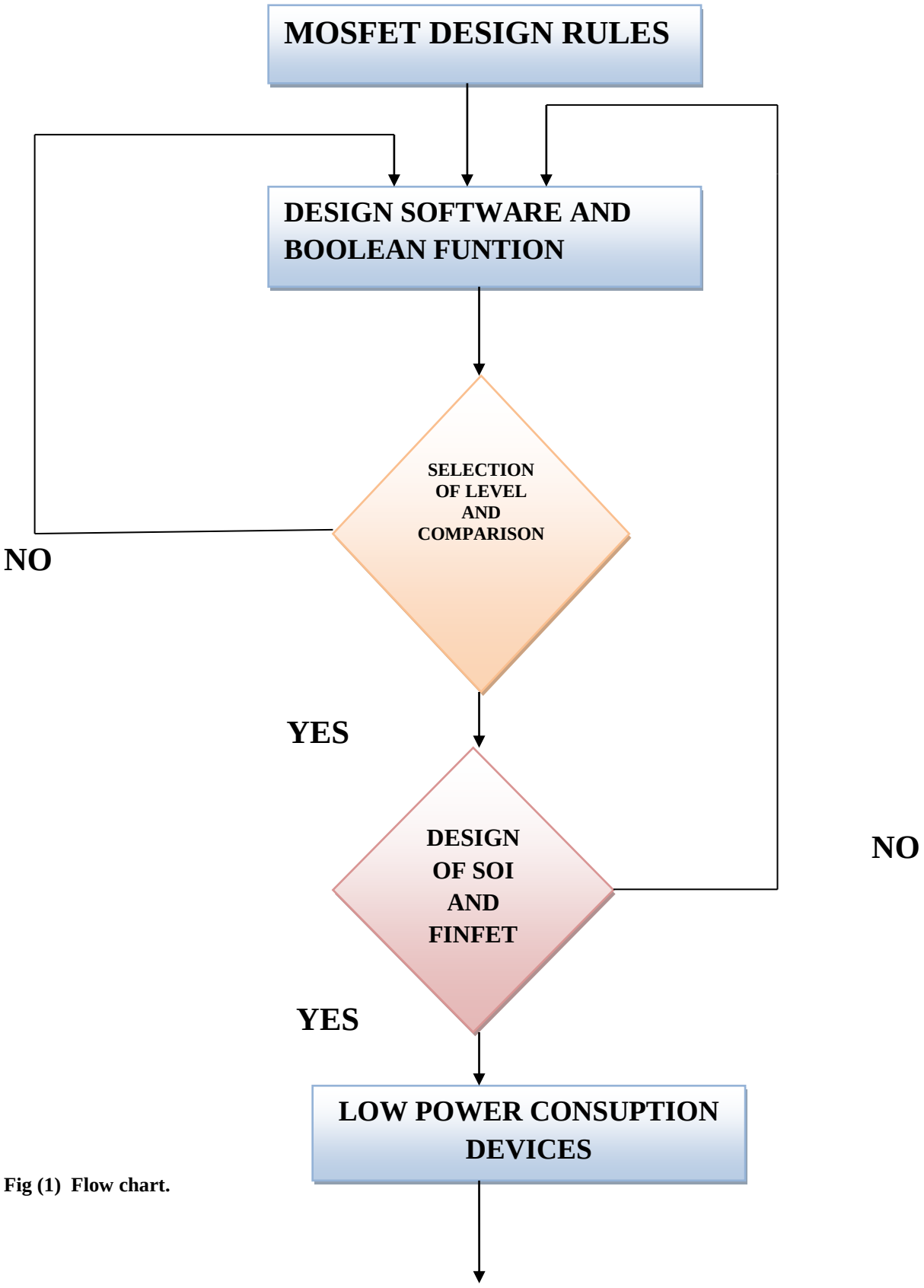


Fig (1) Flow chart.

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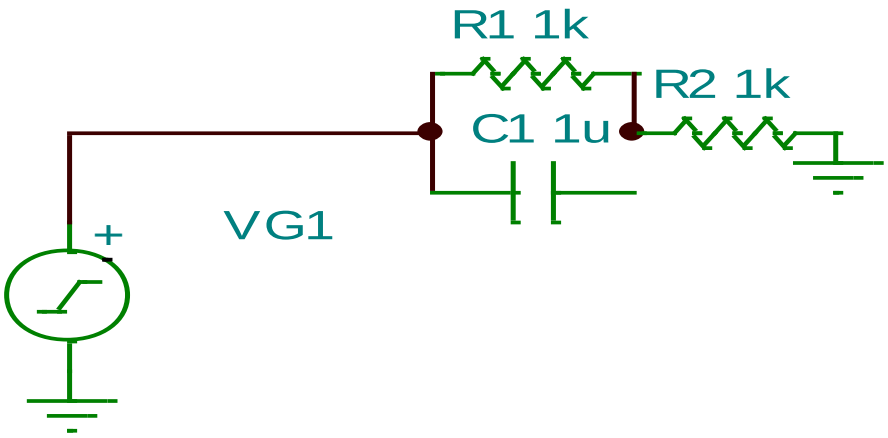


*Fig (2) First-order equalizer.*

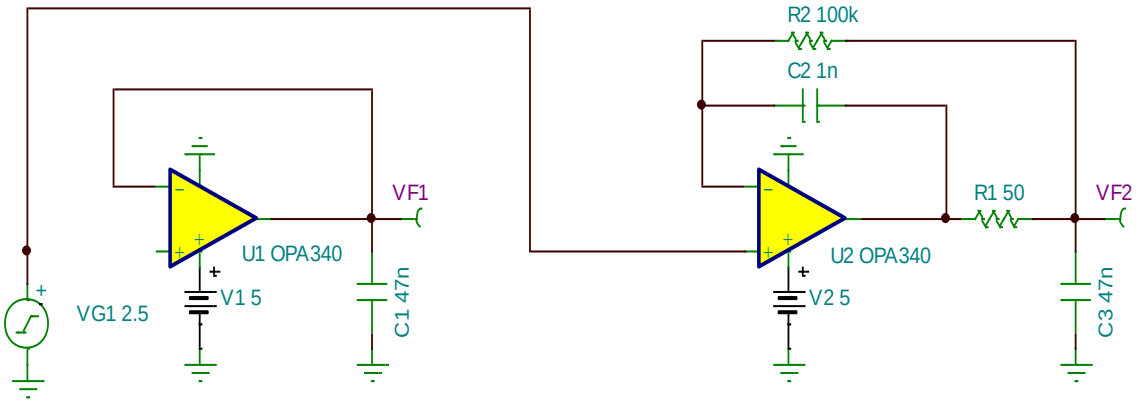


*Fig (3) Small-signal analysis of miller compensation.*

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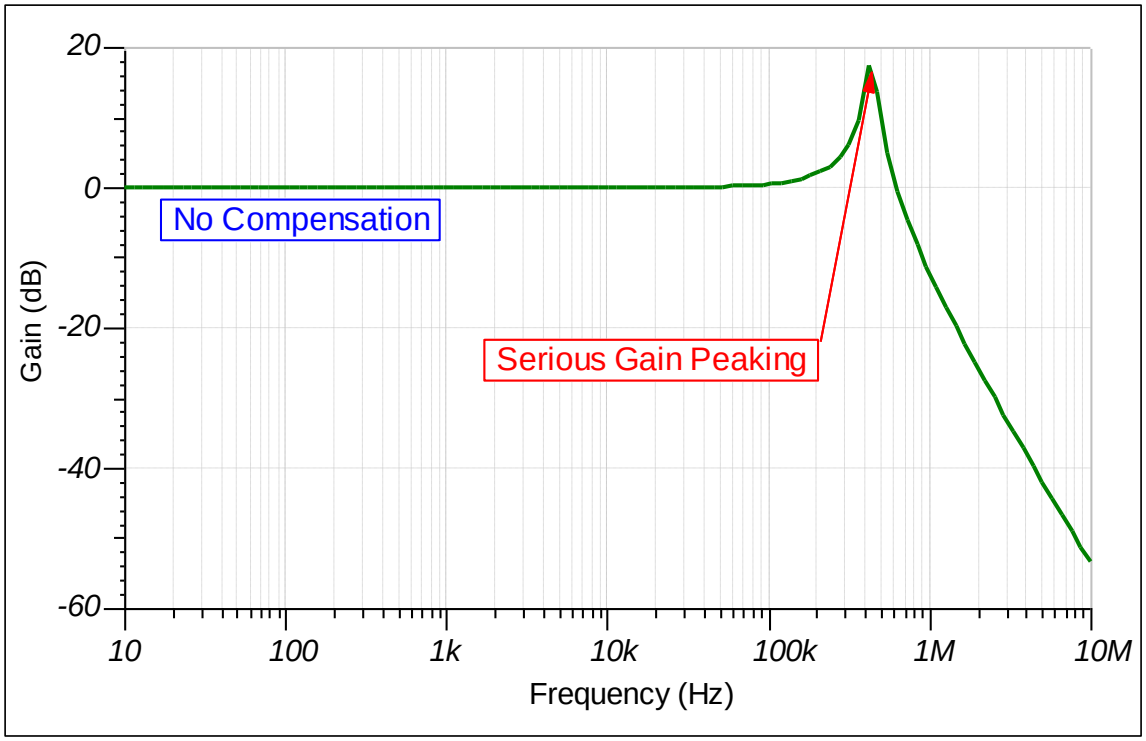


***Fig (4) Gain Vs Frequency Graph.***

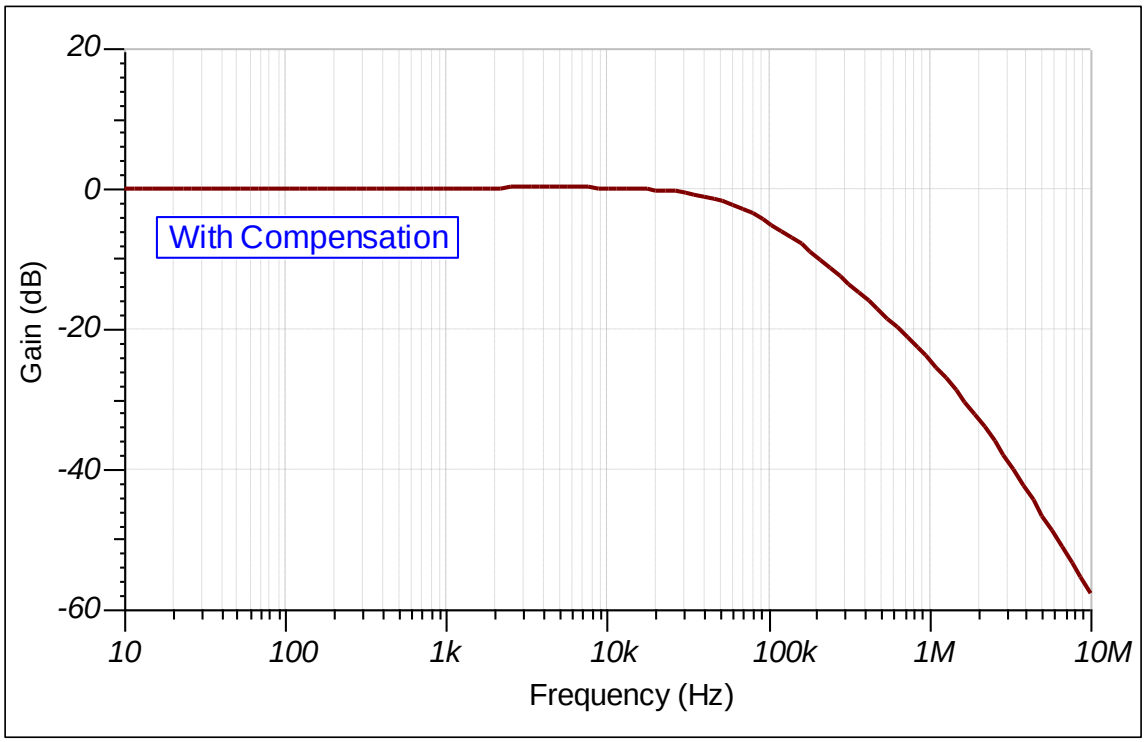


***Fig (5) With compensation.***

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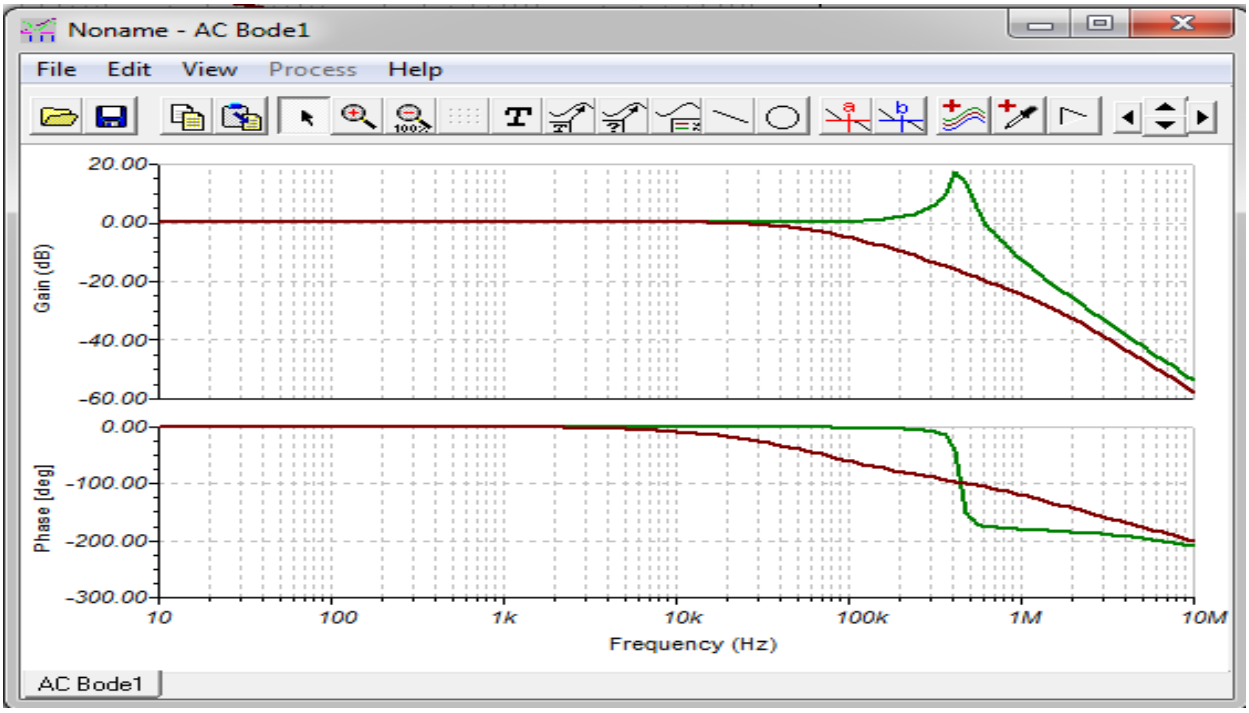


*Fig (6) Comparison between Equalizer and without equalizer output.*

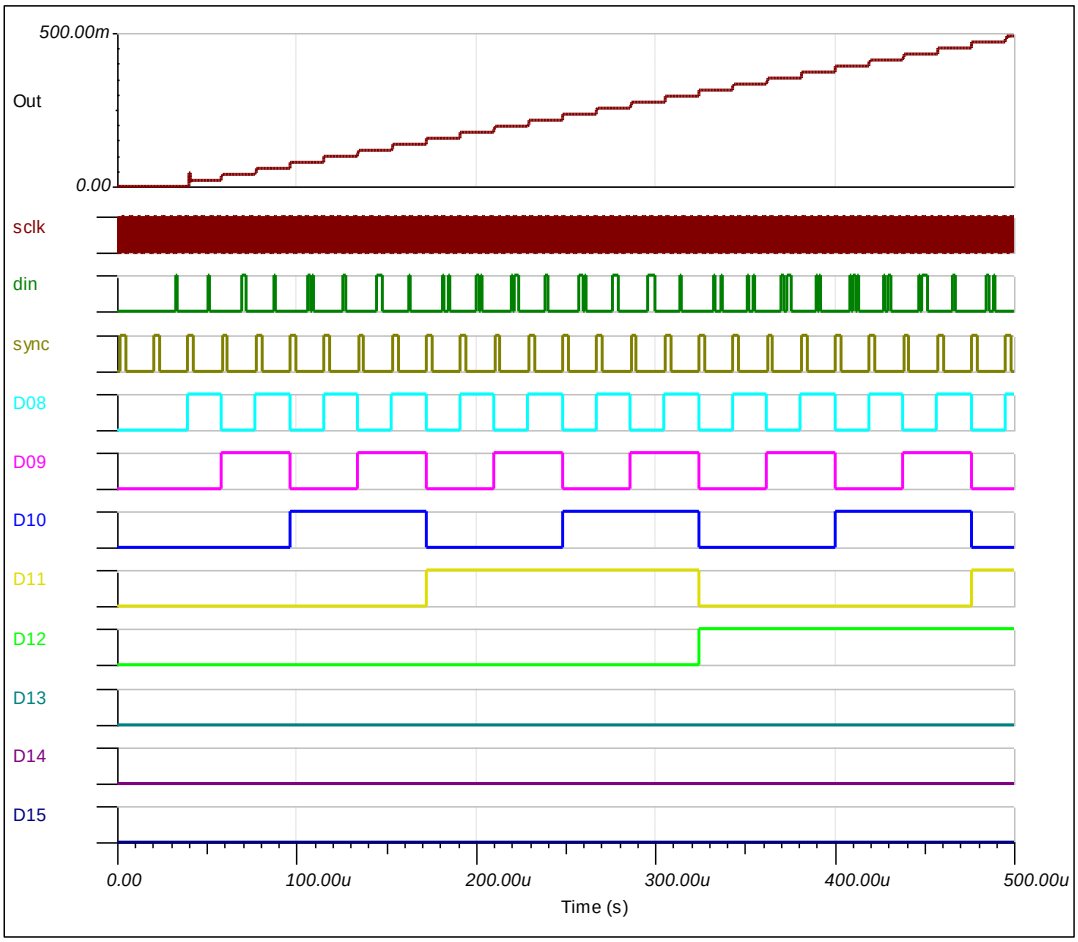


*Fig (7) Analog to digital converter for LED operating.*

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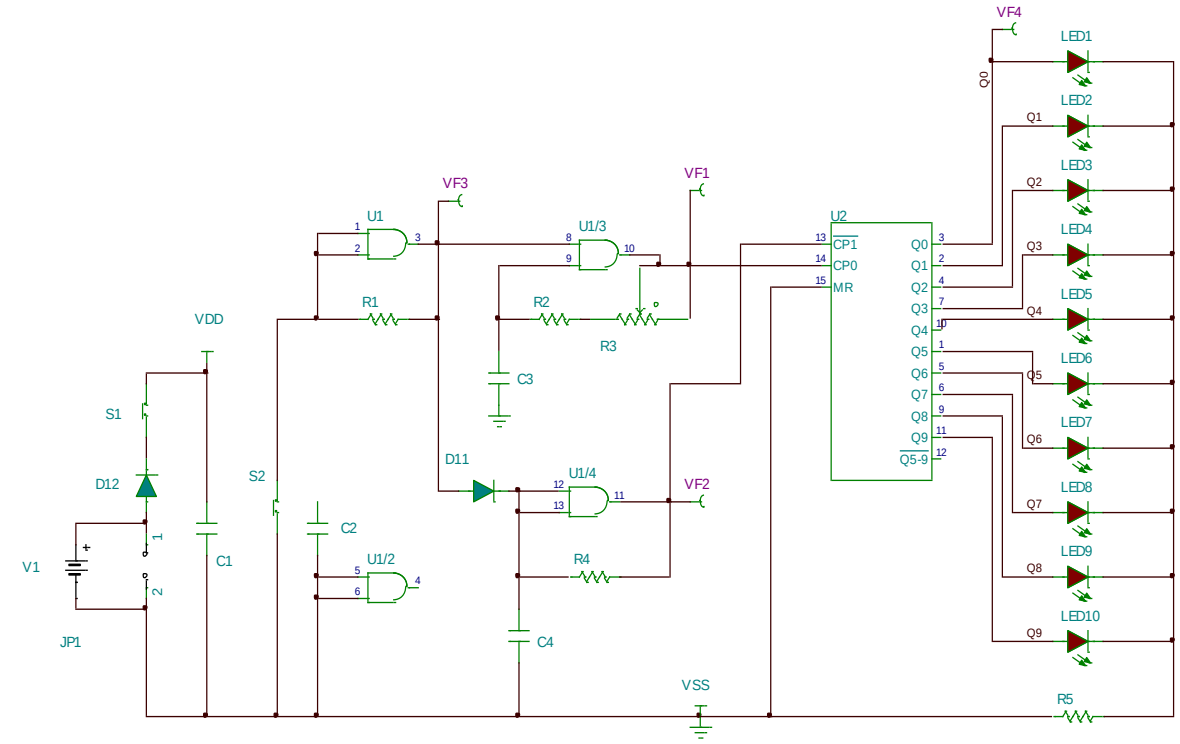


*Fig (8) LED Deriver circuit.*

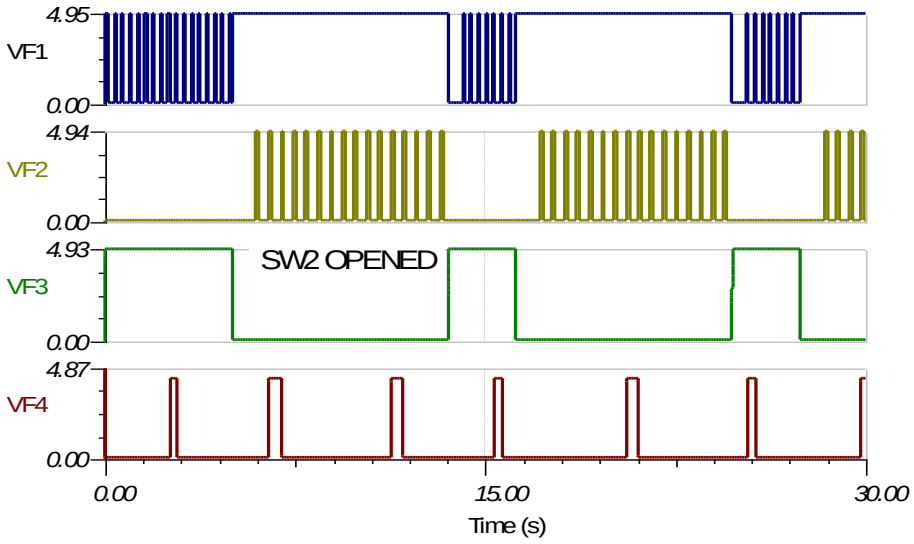


*Fig (9) Output waveform.*

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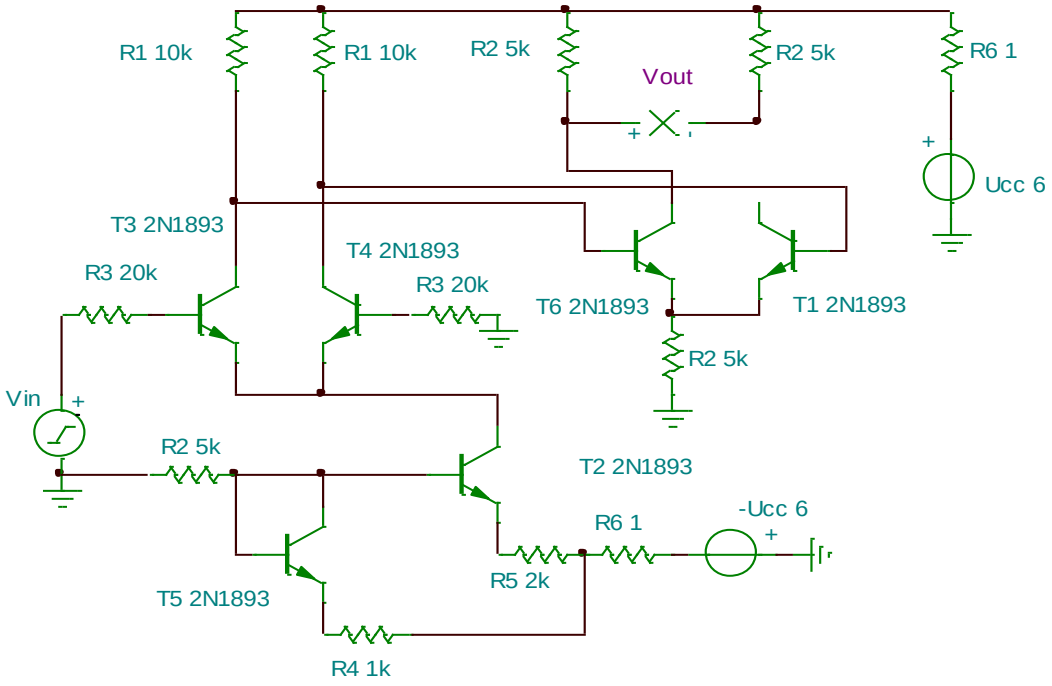


*Fig (10) Differential amplifier.*

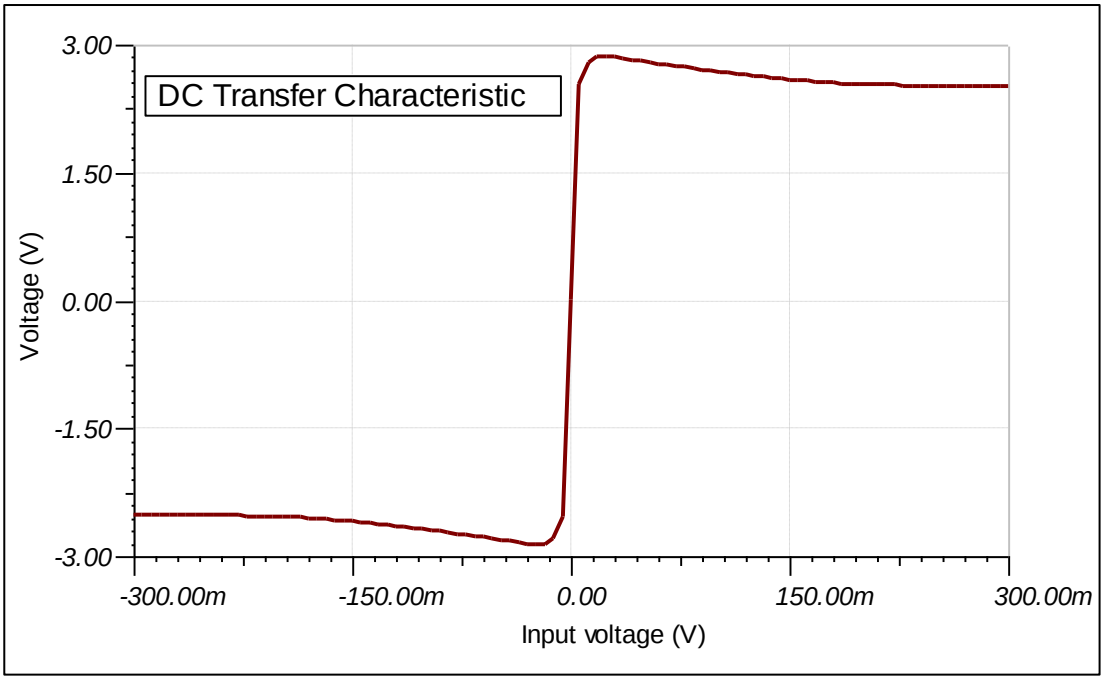


*Fig (11) Transfer characteristics.*

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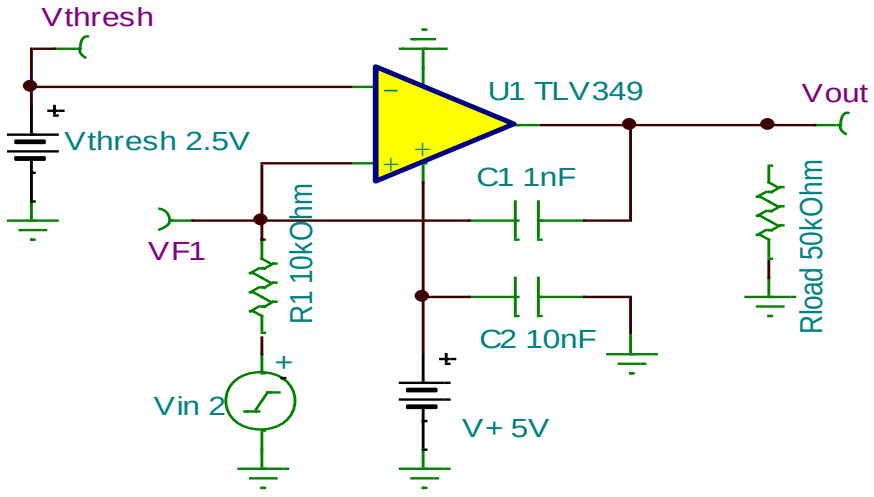


*Fig (12) Level Repeat tore.*

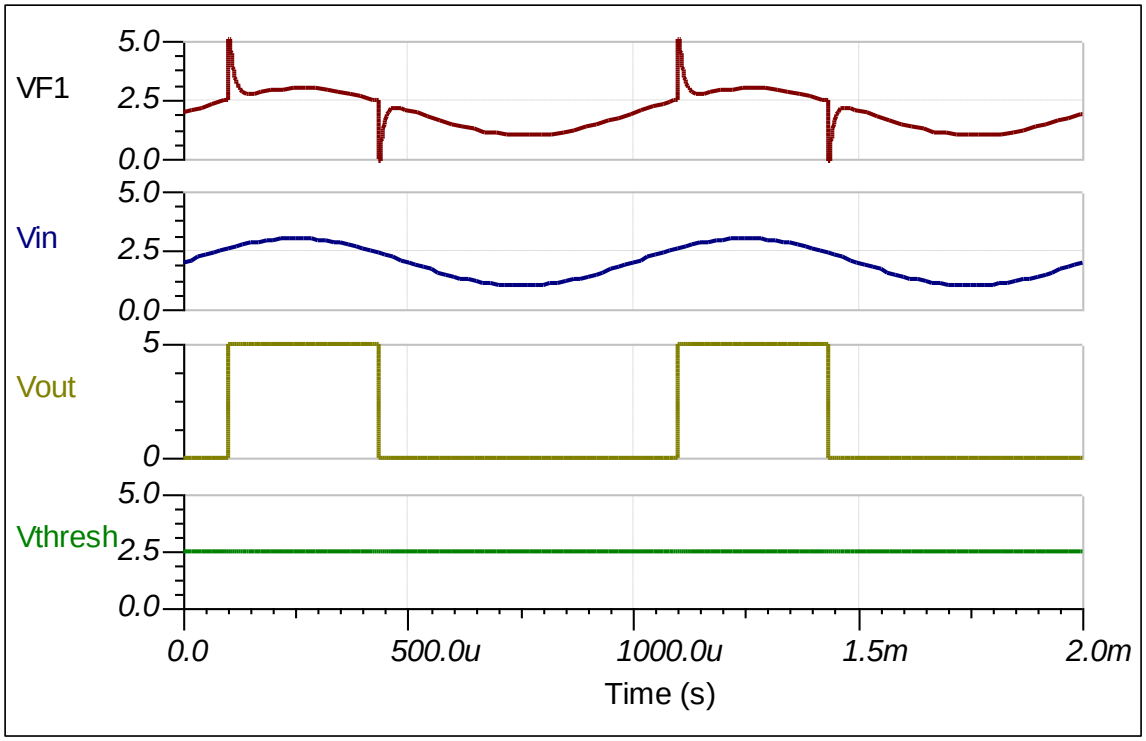


*Fig (6.13) Output wave form.*

**Comparison table Old Vth and Proposed Vth.**

| DESIGN | Vth(old)(v) | (Proposed tech.)Vth(v) |
|---|---|---|
| NAND | 2 | 1.7 |
| NOR | 2.2 | 2.0 |
| RAM | 3.8 | 3.4 |
| ROM | 4 | 3.67 |
| SLICE | 3.2 | 3.2 |
| FLIP FLOP | 3.6 | 3.2 |

## CONCULUSION AND FUTURE WORK

To achieve this goal, a bi-level pulse-width modulation (PWM) driving scheme is applied to enable data transmission during the "OFF" period of the LED drive current. With 3-bit PWM dimming resolution, the driver circuit enables linear luminous intensity control from 5% to 100%. Pseudo-random binary sequences (PRBS) are generated to compare circuit performance for various data modulation formats. The LED driver circuit is simulated in a 0.5μm CMOS process and exhibits a worst-case power consumption of 100mW with 33mA peak PWM current.

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